

exhibit the required current saturation, but there can be technical problems in obtaining good saturation at the necessary current levels of  $2$  to  $3 \times 10^3$  A/cm<sup>2</sup>.

Barrier contacts with poor reverse saturation and contacts with doping notches at the cathode ( $n^+i-n$  or  $n^+p-n$  structures) behave quite differently. These contacts tend to fix the cathode field at a fairly high value throughout the oscillation cycle, and this prevents the device switching to a low-voltage high-current state. In effect, the cathode causes high-field domains to nucleate too readily and the current swing, and hence the efficiency, is low. Curve 2e pertains to a device with a  $1 \mu\text{m}$ ,  $p = 1 \times 10^{15} \text{ cm}^{-3}$  layer between the  $n^+$  cathode and the  $n$ -type active region. The optimum efficiency for this structure is 4%. Very small doping notches can produce small improvements relative to an  $n^+$  contact, but, in general, cathode contacts tending to fix the field at a high value only degrade the efficiency.

In view of these results, the high oscillator efficiencies reported previously<sup>3</sup> are ascribed to hot-electron injection or current-saturation effects or possibly some combination of these.

*Acknowledgment:* This paper is published with the permission of the Director of the Royal Radar Establishment.

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4th December 1974

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#### References

- JONES, D., and REES, H. D.: 'Overlength modes of InP transferred-electron devices', *Electron. Lett.*, 1974, 10, pp. 234-235
- JONES, D., and REES, H. D.: 'Accumulation transit mode in transferred-electron oscillators', *ibid.*, 1972, 8, pp. 566-567
- COLLIVER, D. J., IRVING, L. D., PATTISON, J. E., and REES, H. D.: 'High-efficiency InP transferred-electron oscillators', *ibid.*, 1974, 10, pp. 221-222
- BOERS, P. M.: 'Measurements of the velocity/field characteristic of indium phosphide', *ibid.*, 1971, 7, pp. 625-626
- PREW, B. A.: 'Determination of the velocity/field characteristic for  $n$ -type indium phosphide from dipole-domain measurements', *ibid.*, 1972, 8, pp. 592-594

## TRANSLINEAR CIRCUITS: A PROPOSED CLASSIFICATION

*Indexing terms:* Analogue-computer circuits, Bipolar transistors, Network analysis

An important and expanding branch of analogue circuits is the 'translinear' group. Their primary function arises from the exploitation of the precise proportionality of transconductance to collector current in bipolar transistors so as to result in fundamentally exact, temperature-insensitive behaviour. The basic translinear principle is derived and several examples given.

This letter describes a group of circuits using bipolar transistors and based on a principle that, although fundamental and pervasive, has so far not been formalised. These circuits exploit the linear relationship between transconductance and collector current. This relationship, however, need not appear explicitly in the analysis of translinear circuits. It holds over many orders of magnitude, and is in widespread use in analogue circuits such as multipliers, dividers, squarers, higher-power-function generation, r.m.s. convertors, vector magnitude generators, geometry-correction systems for c.r.t. displays etc. It has also been used to obtain very wideband linear amplification,<sup>1</sup> analogue signal normalisation, sine/cosine synthesis and many other special algebraic operations.

In spite of the importance of these circuits and the common principle they share, there is no noun that defines the group specifically. Such words as 'functional', 'nonlinear', 'processing', 'shaping' etc. are general terms. It is therefore proposed to adopt the coined word 'translinear', defined as follows: a translinear circuit is one having inputs and outputs

in the form of currents and whose primary function arises from the exploitation of the proportionality of transconductance to collector current in bipolar transistors so as to result in fundamentally exact, temperature-insensitive algebraic transformations. The word does not conflict with any existing terms, and conveys the key relationship quite well. The definition is precise, and excludes any circuits based on precision transistors in which the terminal voltages of the devices are used as inputs or outputs, such as logarithmic convertors. Translinear circuits operate entirely in the current domain; voltage variations due to the signals are small, usually tens of millivolts, and are only of incidental interest. The algebraic functions they generate may have many forms, incorporating products, quotients, power terms with fixed exponents, which may be integral or nonintegral, positive or negative, and sums and differences.

Although it is true that these circuits are exact in their processing of signals in the form of currents, they must usually interface with voltage signals. The conversion may incur errors, because voltage variations within the circuits cannot then be ignored. However, precise translinear circuits use operational amplifiers to force collector currents and restore accuracy.

*Translinear principle:* The main distinguishing feature of a translinear circuit is that it uses an even number of forward-biased  $p-n$  junctions arranged in one or more loops, there being as many junctions connected in one polarity direction as in the other. Many circuits have only a single loop, but the principle is general and any number of loops may overlap. Examples of multiple-loop circuits are given below. The junctions are not necessarily the base-emitter junction of a transistor, but, for reasons of accuracy, diodes are not usually

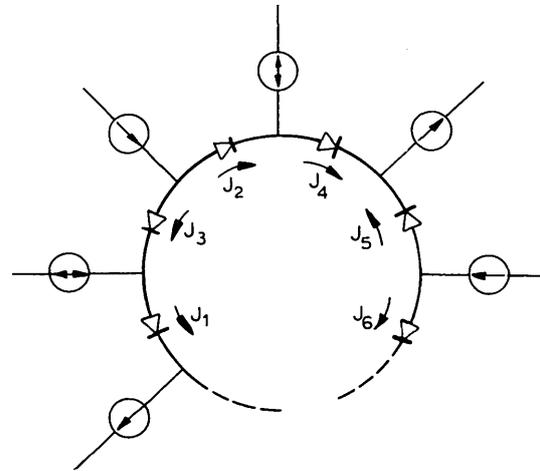


Fig. 1 Generalised single-loop translinear circuit

suitable. Fig. 1 shows a conceptualised single-loop circuit. The currents in the junctions will invariably be set up by 3-terminal connections, but this does not need to be considered in the analysis. Let  $J_r$  be the current density in the  $r$ th junction, and let junctions having clockwise direction be given even suffixes. Summing the voltages around the loop we can write

$$\sum_{r=1}^{N/2} \left( \frac{m_{2r} k T_{2r}}{q} \ln \frac{J_{2r}}{J_0} - \frac{m_{2r-1} k T_{2r-1}}{q} \ln \frac{J_{2r-1}}{J_0} \right) = 0 \quad (1)$$

where  $N$  is the total number of junctions,  $m_r$  is the emission coefficient of the  $r$ th junction,  $kT/q$  is the thermal voltage and  $J_0$  is a scaling constant, which depends on the diffusion profiles and the temperature. Making the assumption that  $m_r$  is the same for all junctions—this is true for transistors operating in their central current range—and assuming that all junctions are at the same temperature, an important requirement of translinear circuits, usually true in monolithic realisations with good layout practice, eqn. 1 reduces to

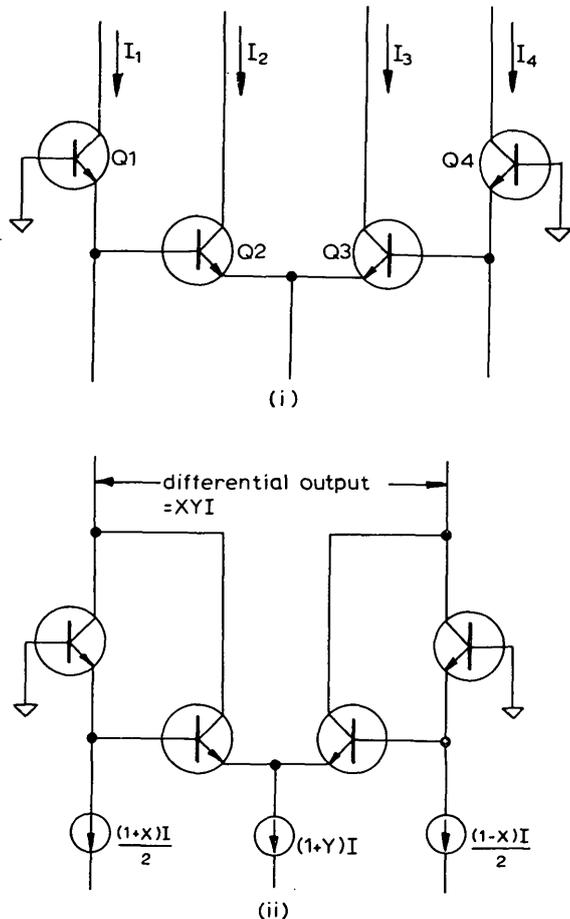
$$\sum_{r=1}^{N/2} (\ln J_{2r} - \ln J_{2r-1}) = 0 \quad \dots \quad (2)$$

Notice that both severely temperature-dependent terms,  $kT/q$  and  $J_0$ , disappear at this step. It is for this reason that

translinear circuits exhibit dramatic insensitivity to isothermal variations of temperature. For the sum of a series of logarithmic terms to be zero the products of the arguments must equal unity. Thus, expressed in its simplest form, the translinear principle states that

$$\prod_{r=1}^{N/2} J_{2r} = \prod_{r=1}^{N/2} J_{2r-1} \dots \dots \dots (3)$$

The simplicity and reliability of this equation makes the synthesis of translinear circuits very rapid. One further step must be taken to make the equation practical: the values for current density must be replaced by actual currents. This reveals that the emitter areas must be precisely controlled to obtain exact operation. The nature and magnitude of the error depends on the specific configuration. It may result merely in a scaling error, or in nonlinearity or departure from the desired transformation. Deliberate mismatch may be



**Fig. 2A**  
 (i) Basic translinear quadruple. The text shows that, for any current levels and temperatures,  $J_1 J_2 = J_3 J_4$   
 (ii) Four-transistor 4-quadrant translinear multiplier

also used to form the function. Local processing variations other than those affecting area, e.g. basewidth, can be described in terms of an equivalent area error, rather than a  $V_{BE}$  error. This has the advantage of being temperature independent, so it can be included in analyses to reveal the overall effect of all such variations on the function. Re-writing eqn. 3 to include emitter areas:

$$\prod_{r=1}^{N/2} \frac{I_{2r}}{A_{2r}} = \prod_{r=1}^{N/2} \frac{I_{2r-1}}{A_{2r-1}} \dots \dots \dots (4)$$

or

$$\prod_{r=1}^{N/2} I_{2r} = \lambda \prod_{r=1}^{N/2} I_{2r-1} \dots \dots \dots (5)$$

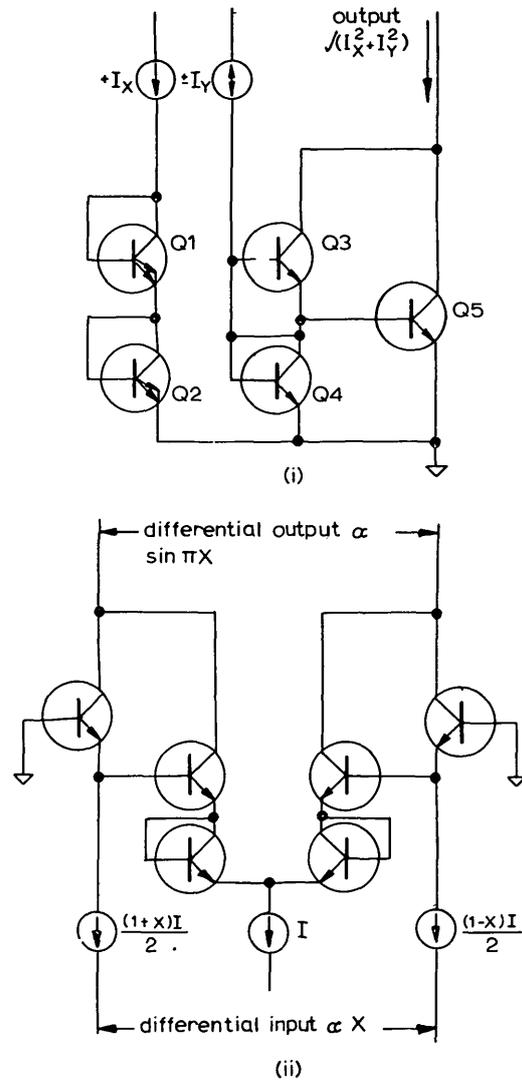
which is identical to eqn. 3 except for the factor  $\lambda$ , which is the 'area factor', for the complete loop, and is given by

$$\lambda = \prod_{r=1}^{N/2} \frac{A_{2r}}{A_{2r-1}} \dots \dots \dots (6)$$

Notice that this factor may still be unity, even though individual areas may depart by any amount from a 'unit' area.

There is no fundamental reason why any of the emitters should have the same area. This can be put to use when designing the layout of monolithic translinear circuits to be insensitive to processing gradients, since, although the individual devices reflect that gradient, they can be arranged so that the net effect on  $\lambda$  is zero. This layout technique invariably results in the lowest sensitivity to thermal gradients for similar reasons.

The analysis of multiple-loop circuits does not present any new problems and proceeds along similar lines to that used in mesh analysis of classical linear networks, and, like them, the



**Fig. 2B**  
 (i) Two-quadrant vector magnitude circuit. Note that the emitter areas of  $Q_1$  and  $Q_2$  are twice that of  $Q_3$ ,  $Q_4$  and  $Q_5$   
 (ii) Sine-approximation circuit. The output is of the form  $X(1-X^2)/(1+X^2)$ , and  $-1 < X < +1$

circuit equations require simultaneous solution when loops are interdependent. The classic translinear circuit<sup>1</sup> is the quadruple of transistors [Fig. 2A(i)]. It may be used as a multiplier, divider, squarer, square-rooter, r.m.s. convertor etc., depending simply on the driving method. For example, when  $I_1$ ,  $I_2$  and  $I_4$  are forced, the output is  $I_3 = I_1 I_2 / I_4$ . If  $Q_2$  is connected as a diode,  $I_2 = I_1 = I$ , so  $I_3 = I^2 / I_4$ . If now  $I_4$  is made equal to the mean value of  $I_3$ , a loop is set up that forces the result  $I_4 = \text{r.m.s.}(I)$ . A surprising number of other functions can be generated with this simple circuit. Many use differential current drive, such as the now standard transconductance multiplier. A simple rearrangement of the circuit provides 4-quadrant multiplication with only four transistors [Fig. 2A(ii)].

Fig. 2B(i) shows a circuit that computes vector magnitude in two dimensions. This is a good example of the extraordinary power of the principle embodied in eqn. 4, by means of which this circuit can be analysed within three or four lines of algebra. It must also represent a very high utilisation efficiency of devices, since only five transistors perform two squaring operations, an addition and a square-root operation.

Fig. 2B(ii) is another 2-loop circuit that generates a very good approximation to the sine function over  $-\pi < \phi < +\pi$ , with an accuracy of  $\pm 0.4\%$  of f.s. when the fixed bias current is made slightly different to  $I$ .

Only a few of the hundreds of translinear variants that have been devised can be shown here. There is a very real need for identifying the basic principle in written and verbal communication, for which none of the prevalent nouns are adequate.

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9th December 1974

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Reference

1 GILBERT, B.: 'A new wideband amplifier technique', *IEEE J. Solid-State Circuits*, 1968, SC-3, pp. 353-365

**SIMPLIFIED METHOD FOR ESTABLISHING DETERMINACY IN A DIRECTED-GRAPH CONTROL STRUCTURE**

Indexing terms: Computer-aided design, Digital systems

The only analytical method so far proposed for establishing determinacy in a model for parallel computation is due to Karp and Miller. It involves growing a tree of every machine state, which is typically very large and needs much computation. The letter describes a very much simpler method suitable for nonpipelined hardware.

It is generally accepted that conventional design techniques for digital systems constitute an art rather than an exact science. Research currently in progress at the Heriot-Watt University involves an attempt to increase the scientific content of these techniques by the construction of an analytical c.a.d. system for parallel digital devices. This system is based on theoretical work on parallel program schemata<sup>1</sup> and is related to the LOGOS project at CWRU.<sup>2</sup>

Essentially, digital devices are modelled as a pair of directed graphs, one (the control graph) defining the flow of control (through a series of special control operators) and the other showing data flow (data graph; details of the graph pair and

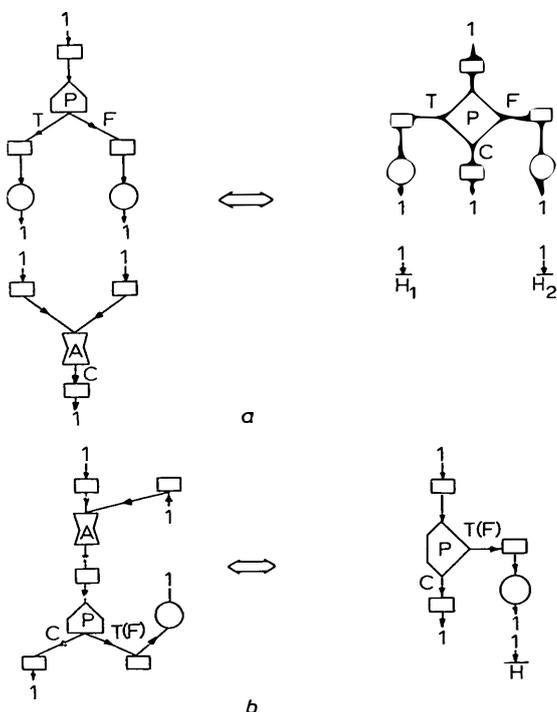
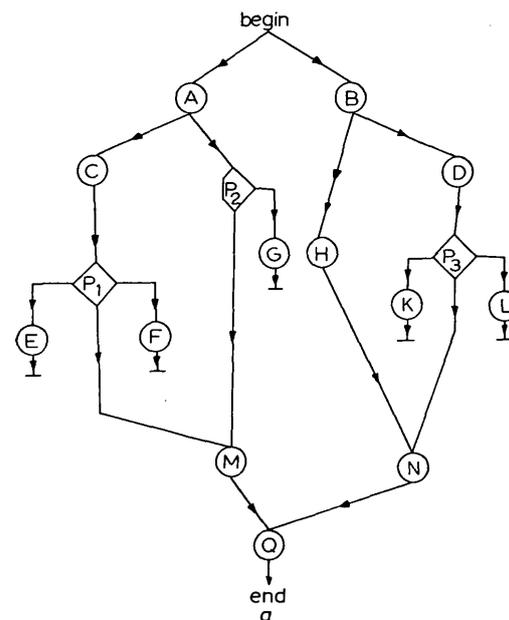


Fig. 1

operators may be found in Reference 3). At present, the analysis requires the construction of the reachability set of a vector addition system<sup>1</sup> and thence the identification of all pairs of operators that may be active simultaneously. In practice, it is found that this theoretically elegant construction consumes large amounts of computer time and space. However, it has been found that this expensive construction can be avoided by suitable structuring of the control graph. This is done by restricting the use of PREDICATE and OR control operators<sup>3</sup> to the configurations shown in Figs. 1a and b (left-hand graphs). Moreover, these structures are identical to control operators defined by Dennis at MIT<sup>4</sup> (right-hand graphs). The mode of operation is, briefly, as follows:

Fig. 1a: On the basis of some data value,  $P$  directs control to path  $T$  or path  $F$ . Subsequently, control passes to path  $C$  via  $A$  (left graph) or  $H_1$  or  $H_2$  (right graph).

Fig. 1b: On the basis of some data value,  $P$  directs control to path  $C$  or  $T(F)$ . If path  $T(F)$  is chosen, control returns to  $P$  via  $A$  (left graph) or  $H$  (right graph).



begin

	B	A	C	D	H	M	N	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	Q	end
begin		1	1									
A												
B			1									
C												
D					1							
H						1						
M											1	
N												1
P <sub>1</sub>								1				
P <sub>2</sub>									1			
P <sub>3</sub>										1		
Q												1
end												

'blank'=0

begin

	B	A	C	D	H	M	N	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	Q	end
begin		1	1	1	1	1	1	1	1	1	1	1
A			1					1	1	1	1	1
B												
C										1	1	1
D											1	1
H												1
M												1
N												1
P <sub>1</sub>									1			
P <sub>2</sub>										1		
P <sub>3</sub>											1	
Q												1
end												

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Fig. 2